REMARKS

Claims 1-19 are currently pending in the application. By this amendment, claims 1, 4 and 7 are amended for the Examiner's consideration. The foregoing separate sheets marked as "Listing of Claims" shows all the claims in the application, with an indication of the current status of each .

The Examiner's acceptance of the drawings is acknowledged.

The Examiner has rejected claims 1, 3, 4, 6, 7, 9, 10 and 14 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application No. 2003/0128080 to Viswanathan et al. ("Viswanathan"). Viswanathan discloses an electronic component 100 having a carrier substrate 110 and an electronic device 130, such as a semiconductor chip, on the substrate 110. The electronic device 130 is housed within cavity 160. Further, the electronic device 130 and the carrier substrate 110 are covered by a cover 140, which comprises many layers with conductor tracks 145, 146, 147 extending transversely through the plurality of layers. The carrier substrate 110 functions as a heat sink, supplemented by heat sink 230. The electronic connection for the module 100 is provided on the upper surface of the cover 140, opposite to the carrier substrate 110. The electronic device 130 is built into the cavity 160 using flip-chip technology, and is connected via substrate 110 to heat sink 230. Substrate 110 is comprised of copper tungsten with surface coatings of nickel and gold to provide a solderable surface (¶0017). The substrate 120 for device 130 can have a backmetal 122 forming a eutectic bond between device substrate 120 and carrier substrate 110 by heating the backmetal 122 (¶0020). Note that backmetal 122 is less than two microns thick and serves no electrical function, the electrical function being provided by connectors 142 at the side opposite the backmetal or by electrical leads 450 from the side, as shown in Figures 2 and 4. Note further that connectors 142 connect to printed-circuit-board 220 as shown in Figure 2, and that these connections to the circuit board 220 are on the opposite side of cover 140 from the cavity 160 and the electronic device 130.

This orientation is exactly the reverse of that claimed for the present invention. The explanation for this reversal – which completely distinguishes the Viswanathan reference – is the manner in which heat dissipation for the electronic device is provided. Viswanathan provides heat dissipation using the carrier substrate 110 and heat sink 230 located away from the circuit board, on the opposite side of cover 140. By contrast, the present invention uses the filling material to provide a heat dissipation path to the circuit board (page 8, lines 8-12), leaving the side away from the circuit board free for providing additional components.

The independent claims have been amended to clarify this distinction in orientation of claimed elements between the Viswanathan reference and the present invention.

In addition, it should be emphasized that Viswanathan provides no teaching of a single structure (here, the filling material) providing the functions of heat dissipation, electrical connectivity and insulation by one step construction, and a hermetic seal by encapsulation of the semiconductor chip within a cavity.

It should be noted that the use of the filling material as described in the present invention enables a more compact structure which is less expensive to manufacture and more integrated (page 3, lines 26-34). The further attributes and advantages of the filling material are described in dependent claims.

The Examiner has rejected claims 2, 8, 12, 13, 15 and 16 under 35 U.S.C. §103(a) as being unpatentable over Viswanathan in view of U.S. Patent Application No. 2003/0071350 to Takehara et al. ("Takehara"). Since, as shown above, Viswanathan fails to provide a valid reference as to the independent claims, Takahara's use of a resin cannot overcome the deficiency of Viswanathan. Further, the resin material disclosed in Takehara is completely filled into the cavity, which is not in accordance with the limitation of the present invention which does not enclose the connecting contacts and bumps.

The Examiner has rejected claims 5 under 35 U.S.C. §103(a) as being unpatentable over Viswanathan in view of U.S. Patent No. 6,384,701 to Yamada et al. "Yamada"). The Examiner has rejected claims 11 and 17-19 under 35 U.S.C. §103(a)

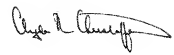
as being unpatentable over Viswanathan in view of U.S. Patent No. 5,064,782 to Nishiguchi. Since the Viswanathan reference has been shown above to fail as a reference with respect to the independent claims, these additional grounds of rejection are also overcome.

In view of the foregoing, it is requested that the application be reconsidered, that claims 1-19 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at 703-787-9400 (fax: 703-787-7557; email: clyde@wcc-ip.com) to discuss any other changes deemed necessary in a telephonic or personal interview.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Sincerely,



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